

OR3 - ATT3.2

Baseband Receiver chip architecture specification

TorinoWireless, Accent, Novasis

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Base band chip specifications

Evolution of BB: full custom chipset

Target technology:

- SMIC 0.13um, same as RF

SOC Fabric:

- ARM 926EJ hard macro available from SMIC
- PLL & embedded memories hard macros available from SMIC
- ARM Primecell IPs for AHB standard peripherals

GPS related IPs

- Custom design for tracking
- Custom design for acquisition



Base band chip specifications



Evolution of BB: Atmel

Commercial product name: AT91CAP

- AT91SAM SOC + 500K gates user customizable area
- 0,13um ATMEL process

☐ SOC Fabric:

- Pre-verified AT91SAM SOC
- ARM 926EJ processor
- Atmel Standard peripheral set
- SRAM and DPRAM blocks available

☐ GPS IPs:

- To be mapped in the user customizable area
- Custom design



Base band chip specifications



Evolution of BB: Altera

Altera:

- FPGA solution (Stratix devices)
- Hardcopy device possible (structured ASIC implementing custom blocks and ALTERA IPs)

SOC Fabric:

- ALTERA NIOS embedded processor and peripheral set

GPS IPs:

- Custom design
- Accelerated using ALTERA IPs such as CORDIC, FFT



Base band chip specifications



Evolution of BB: Xilinx

Xilinx:

- FPGA solution (Virtex devices)
- Easypath device possible (FPGA tested using customer bitstream)

SOC Fabric:

- XILINX MICROBLAZE embedded processor and peripheral set

GPS IPs:

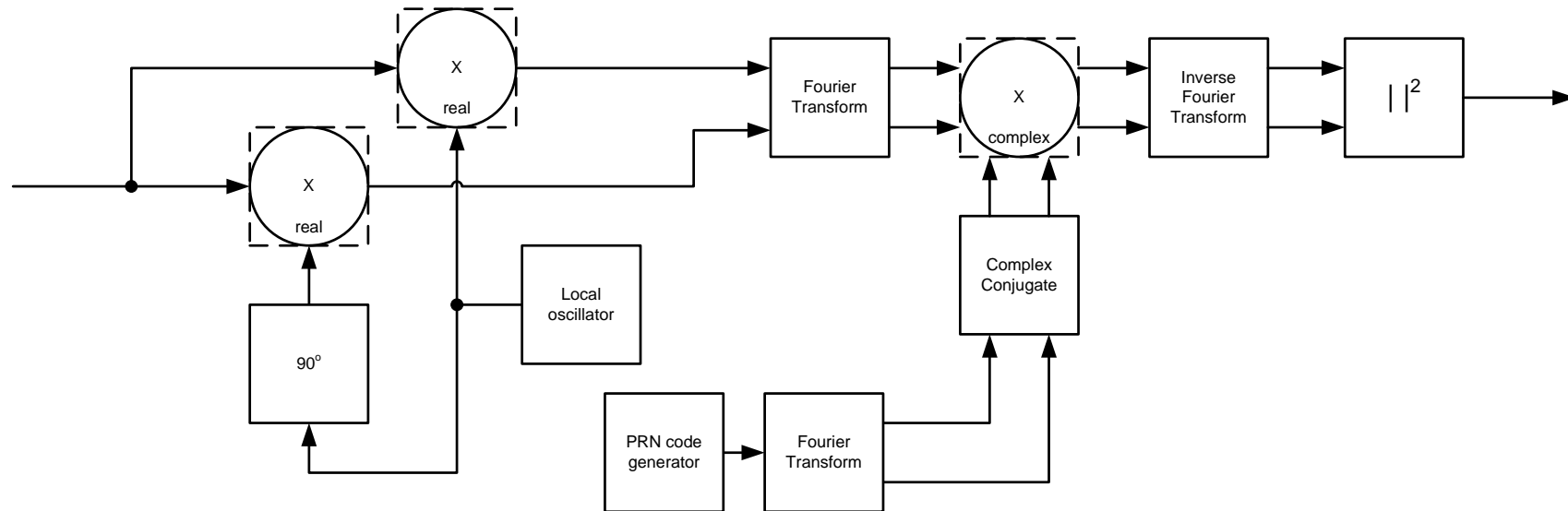
- Custom design
- Accelerated using XILINX IPs such as CORDIC, FFT



Base band chip specifications



Acquisition Algorithm: block diagram



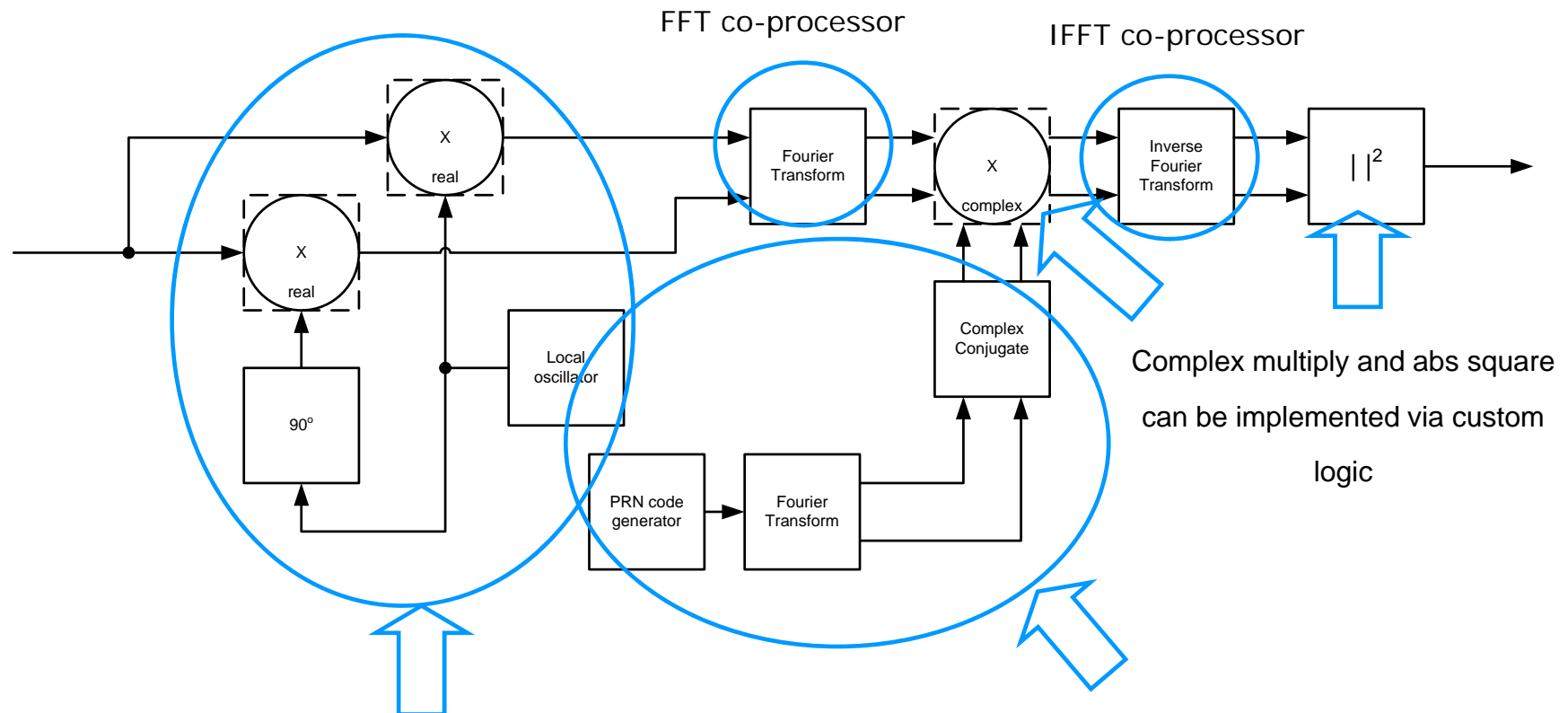
- ❑ Critical in GPS/Galileo receivers, due to high computational time
- ❑ Recently faster algorithms working in the frequency domain have been proposed (parallel code phase search acquisition)
- ❑ The main drawback is the hardware overhead, with respect to traditional acquisition schemes
- ❑ Highly integrated technologies can overcome the problem



Base band chip specifications



Acquisition Algorithm: hw implementation (1)



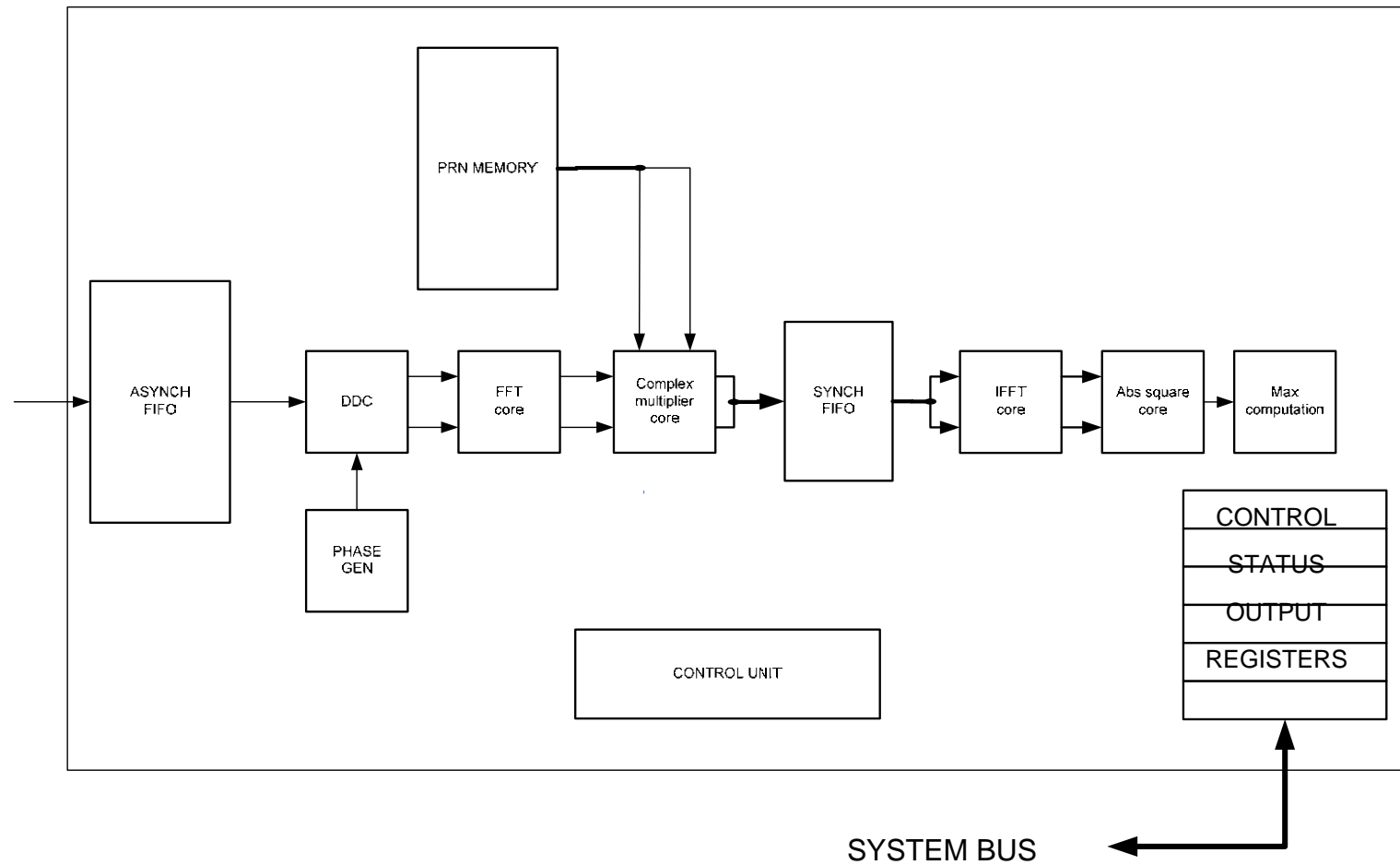
In phase and Quadrature components can be generated using a DDC implemented by a cordic core, controlled by a phase generator to account for doppler effect

This branch can be stored in memory, as the PRN code depends only on the search satellite



Base band chip specifications

Acquisition Algorithm: hw implementation (2)





Base band chip specifications



Acquisition Algorithm: hw implementation - facts

- The input async. FIFO is used to speed up the clock frequency with respect to the input data rate.
- Maximum clock frequency is limited by combinational logic but mainly by the transfer time of the PRN memory (can be internal or external, or a mixed solution).
- DDC and phase generator precision are dependent on the frequency drift that needs to be corrected (doppler shift)
- FFT and IFFT core are duplicated to allow a better parallelism (faster execution time)
- The synch FIFO is used to overcome the latency of the IFFT core
- The most critical cores are the FFT and the IFFT which should work on a large number of samples in a streaming architecture



Acknowledgements

This research has been performed in the framework of the IRGAL Project
(Innovation and Research on GALileo)
co-funded by the European Union, the Italian Ministry of Economy and
Finance and the Piedmont Region within the DOCUP 2000-2006,
mis. 3.4 Programme.



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